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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/451,619	11/30/1999	SEIICHI MORI	005702-20050	9292
26021	7590	07/02/2004	EXAMINER	
HOGAN & HARTSON L.L.P. 500 S. GRAND AVENUE SUITE 1900 LOS ANGELES, CA 90071-2611			WEISS, HOWARD	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/451,619

Applicant(s)

MORI, SEIICHI

UK

Examiner

Howard Weiss

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 April 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 4,6,19-22 and 24 ~~is/are~~ are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 4,6,19-22 and 24 ~~is/are~~ are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

Attorney's Docket Number: 005702-20050  
Filing Date: 11/30/99  
Continuing Data: none  
Claimed Foreign Priority Date: 11/30/98 (JPX)  
Applicant(s): Mori

Examiner: Howard Weiss

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 4 adds the limitation of an electric charge accumulating portion in an insulating layer having a trap level. This charge accumulating insulating layer is in addition to the floating gate described in Claim 19 from which Claim 4 depends. There is no description in the specification nor depiction in the figures of this arrangement.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al. (U.S. Patent No. 6,130,452) and Kume et al. (IEDM 87).

Lu et al. show most aspects of the instant invention (e.g. Figure 1 and Column 5 Lines 15 to 41 ) including:

- a semiconductor substrate **104**
- a source region **120** and a drain region **118a**
- a floating gate **100, 108** provided on an insulating layer **102**
- the overlap **124a** of said drain region with the floating gate is larger than the overlap **124b** of said source region
- the erasing and writing procedures are as claimed (Column 4 Line 27 to Column 5 Line 13) including using hot electron injection (Column 5 Lines 5 to 7)
- the ends of the source and drain regions **124a,b** are in predetermined positional relations with sidewalls **106a,b**

Lu et al. do not show the source junction depth being larger than the drain junction depth. Kume et al. teach (e.g. Figure 1) to have the source junction depth (the boundary between the n- layer of the source region and the p substrate) larger than the drain junction depth (the boundary between the n+ drain region and the p+ layer) to improve programming efficiency (Page 560 Column 2 second paragraph). It would have been obvious to a person of ordinary skill in the art at the time of invention to have the source junction depth larger than the drain junction depth as taught by Kume et al. in the device of Lu et al. to improve programming efficiency.

5. Claims 4, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al. and Kume et al., as applied to Claim 19 above, and in further view of Okuda et al. (U.S. Patent No. 5,640,345).

Lu et al. and Kume et al. show most aspects of the instant invention (Paragraph 7) except for a electric charge accumulating portion in an insulating layer having trap level replacing the floating gate. Okuda et al. teach (e.g. Figures 1(a,b)) to a electric charge accumulating portion in an insulating layer having trap levels **11, 12, 14,15** to

provide a low-voltage and high data performance device (Column 2 Lines 52 to 61). It would have been obvious to a person of ordinary skill in the art at the time of invention to a electric charge accumulating portion in an insulating layer having trap levels as taught by Okuda et al. in the device of Lu et al. and Kume et al. to provide a low-voltage and high data performance device.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al. and Kume et al., as applied to Claim 19 above, and in further view of Sung et al. (U.S. Patent No. 5,631,179).

Lu et al. and Kume et al. show most aspects of the instant invention (Paragraph 7) except for the a side wall on said control gate made of two layers. Sung et al. teach (e.g. Figures 1A and 3A) to have the side wall on the control gate **14** to have two layers **28, 29'** to reduce the number of source pickups (Column 1 Lines 28 to 30). It would have been obvious to a person of ordinary skill in the art at the time of invention to have the side wall on the control gate to have two layers as taught by Sung et al. in the device of Lu et al. and Kume et al. to reduce the number of source pickups.

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al., Kume et al. and Okuda et al., as applied to Claim 21 above, and in further view of Sung et al.

Lu et al., Kume et al. and Okuda et al. show most aspects of the instant invention (Paragraph 8) except for the a side wall on said control gate made of two layers. Sung et al. teach (e.g. Figures 1A and 3A) to have the side wall on the control gate **14** to have two layers **28, 29'** to reduce the number of source pickups (Column 1 Lines 28 to 30). It would have been obvious to a person of ordinary skill in the art at the time of invention to have the side wall on the control gate to have two layers as

taught by Sung et al. in the device of Lu et al., Kume et al. and Okuda et al. to reduce the number of source pickups.

### ***Response to Arguments***

8. The Applicant's arguments filed 3/13/03 have been fully considered but they are not persuasive. In reference the limitations of Claim 4, a dependent claims has all the limitations of the base, or independent, claim plus the limitations stated in the dependent claim and any intervening claims. In this case, Claim 4 adds an electric charge accumulating, trap level insulating layer to the memory cell device. This is in additions to a floating gate (Claim 19). In the description and figures referenced by the Applicants, the floating gate **4** and inter-layer insulating layer **5** (Figure 2F) are replaced by an ONO layer **20** (Figure 3). Therefore, the claimed invention of Claim 4 has a different structure than that described in the Specification and shown in the figures.

In reference to the claim language referring to how the writing operation is executed, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In the instant case, The memory device of the combination of the prior art has all the structure including the main features of the drain region overlap larger than the source region overlap and the junction depth of the source region larger than the junction depth of the drain region. Additional, Lu et al. state that the device may be programmed and erased by any of a number of methods (Column 5 Lines 5 to 7) which would included those claimed.

In reference to the rejection not addressing the problem confronted by the claimed invention, the mere fact that the references relied upon by the Examiner to evince an appreciation of the problem identified and solved by the instant invention is not, standing alone, conclusive evidence of the non-obviousness of the claimed subject matter. The references may suggest doing what an applicant has done even though those of ordinary skill in the art were ignorant of the existence of the problem. *In re Gershon*, 152 USPQ 602 (CCPA 1967).

In response to applicant's argument that the two layer sidewalls of Sung et al. cannot be used to produce self-aligned ion implantation, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In view of these reasons and those set forth in the present office action, the rejections of the stated claims stand.

### **Conclusion**

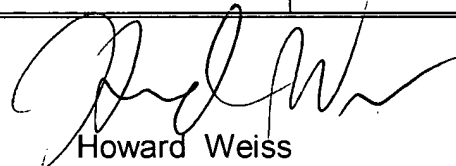
9. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 872-9306**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(571) 272-1720** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via **Howard.Weiss@uspto.gov**.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 Receptionist at **(703) 308-0956**.

11. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/ 315, 324; 438/288	thru 6/24/04
Other Documentation: none	
Electronic Database(s): EAST (USPAT)	thru 6/24/04

HW/hw  
24 June 2004

  
Howard Weiss  
Examiner  
Art Unit 2814